Claims

What is claimed is:

1. A method of constructing a structural model for a memory for use in ATPG (Automatic Test Pattern Generation), said method comprising the steps of:

accessing a simulation model of said memory from a simulation library stored in memory of a computer system, said simulation model described in a behavioral hardware description language;

generating a simplified behavioral model of said memory by re-describing said memory with a predefined subset of said behavioral hardware description language; and

under computer control, automatically translating said simplified behavioral model into said structural model of said memory and storing said structural model in said memory wherein said structural model comprises a plurality of ATPG memory primitives.

2. A method as recited in Claim 1 wherein said simplified behavioral model excludes timing information contained in said simulation model of said memory.

3. A method as recited in Claim 2 further wherein said simplified behavioral model excludes physical layout information contained in said simulation of said memory.

4. A method as recited in Claim 1 wherein said plurality of ATPG memory primitives each represents a functionality of said memory.

5. A method as recited in Claim 4 wherein said plurality of ATPG memory primitives comprises: a memory primitive; an address bus primitive; a data bus primitive; a read port primitive; and a plurality of macro output primitives.

6. A method as recited in Claim 4 wherein said memory is a random access memory (RAM) and wherein said plurality of ATPG memory primitives comprises:

an address bus primitive;

a memory primitive for coupling to receive addresses from said address bus primitive;

a data bus primitive for coupling to provide data to said memory primitive;

a read port primitive for coupling to receive data from said memory primitive and for coupling to receive addresses from said address bus primitive; and

a plurality of macro output primitives for coupling to said read port.

7. A method as recited in Claim 4 wherein said plurality of ATPG memory primitives comprises: a memory primitive; a compare port primitive; and a plurality of macro output primitives.

8. A method as recited in Claim 4 wherein said memory is a content addressable memory (CAM) and wherein said plurality of ATPG memory primitives comprises:

a memory primitive;

a compare port primitive for coupling to receive first data from a data bus primitive and for coupling to said receive second data from said memory primitive, wherein said compare port primitive is for comparing said first data and said second data and for supplying an address of said memory primitive provided said first data matches said second data; and

a plurality of macro output primitives for outputting said address of said memory primitive.

9. A method as recited in Claim 1 further comprising the step of verifying functional equivalence between said simplified behavioral model and said simulation model by applying both models to a behavioral hardware description language simulator.

10. A method as recited in Claim 1 wherein said behavioral hardware description language is Verilog.

11. A method as recited in Claim 1 wherein said behavioral hardware description language is VHDL.

12. A method as recited in Claim 1 further comprises the step of displaying a graphical representation of said primitives of said structural model of said memory and their interconnections on a display screen of said computer system.

13. A computer readable medium having computer-readable program code embodied therein for causing a computer system to perform a method of constructing a structural model for a memory for use in ATPG (Automatic Test Pattern Generation), said method comprising the steps of:

accessing a simplified behavioral model of said memory wherein said simplified behavioral model is described in a behavioral hardware description language and wherein said simplified behavioral model is generated based on a simulation model of said memory; and

automatically translating said simplified behavioral model into said structural model for said memory and storing said structural model into a memory of said computer system wherein said structural model comprises a plurality of ATPG memory primitives.

14. A computer readable medium as recited in Claim 13 wherein said simplified behavioral model excludes timing information contained in said simulation model of said memory.

15. A computer readable medium as recited in Claim 14 further wherein said simplified behavioral model excludes physical layout information of said memory.

16. A computer readable medium as recited in Claim 13 wherein said plurality of ATPG memory primitives each represents a functionality of said memory.

17. A computer readable medium as recited in Claim 16 wherein said plurality of ATPG memory primitives comprises: a memory primitive; an address bus primitive; a data bus primitive; a read port primitive; and a plurality of macro output primitives.

18. A computer readable medium as recited in Claim 16 wherein said memory is a random access memory (RAM) and wherein said plurality of ATPG memory primitives comprises:

an address bus primitive;

a memory primitive for coupling to receive addresses from said address bus primitive;

a data bus primitive for coupling to provide data to said memory primitive;

a read port primitive for coupling to receive data from said memory primitive and for coupling to receive addresses from said address bus primitive; and

a plurality of macro output primitives for coupling to said read port.

19. A computer readable medium as recited in Claim 16 wherein said plurality of ATPG memory primitives comprises: a memory primitive; a compare port primitive; and a plurality of macro output primitives.

20. A computer readable medium as recited in Claim 16 wherein said memory is a content addressable memory (CAM) and wherein said plurality of ATPG memory primitives comprises:

a memory primitive;

a compare port primitive for coupling to receive first data from a data bus primitive and for coupling to said receive second data from said memory primitive, wherein said compare port primitive is for comparing said first data and said second data and for supplying an address of said memory primitive provided said first data matches said second data; and

a plurality of macro output primitives for outputting said address of said memory primitive.

21. A computer readable medium as recited in Claim 13 wherein said method further comprises the step of verifying functional equivalence between said simplified behavioral model and said simulation model by applying both models to a behavioral hardware description language simulator.

22. A computer readable medium as recited in Claim 13 wherein said behavioral hardware description language is Verilog.

23. A computer readable medium as recited in Claim 13 wherein said behavioral hardware description language is VHDL.

24. A computer readable medium as recited in Claim 13 further comprises the step of displaying a graphical representation of said primitives of said structural model of said memory and their interconnections on a display screen of said computer system.

25. A computer controlled electronic design automation system comprising:

a processor;

a display device;

a bus coupled to said processor; and

a computer readable medium coupled to said bus and having stored therein computer readable program code for causing said electronic design automation system to perform a method of constructing a structural model for a memory for use in ATPG (Automatic Test Pattern Generation), said method comprising the steps of:

(a) accessing a simplified behavioral model of said memory from said computer readable medium wherein said simplified behavioral model is described in a behavioral hardware description language and wherein said simplified behavioral model is generated based on a simulation model of said memory; and

(b) automatically translating said simplified behavioral model into said structural model of said memory and storing said structural model into said computer readable medium, wherein said structural model comprises a plurality of ATPG memory primitives.

26. A electronic design automation system as recited in Claim 25 wherein said simplified behavioral model excludes timing information of said memory.

27. A electronic design automation system as recited in Claim 26 further wherein said simplified behavioral model excludes physical layout information of said memory.

28. A electronic design automation system as recited in Claim 25 wherein said plurality of ATPG memory primitives each represents a functionality of said memory.

29. A electronic design automation system as recited in Claim 28 wherein said plurality of ATPG memory primitives comprises: a memory primitive; an address bus primitive; a data bus primitive; a read port primitive; and a plurality of macro output primitives.

30. A electronic design automation system as recited in Claim 28 wherein said memory is a random access memory (RAM) and wherein said plurality of ATPG memory primitives comprises:

an address bus primitive;

a memory primitive for coupling to receive addresses from said address bus primitive;

a data bus primitive for coupling to provide data to said memory primitive;

a read port primitive for coupling to receive data from said memory primitive and for coupling to receive addresses from said address bus primitive; and

a plurality of macro output primitives for coupling to said read port.

31. A electronic design automation system as recited in Claim 28 wherein said plurality of ATPG memory primitives comprises: a memory primitive; a compare port primitive; and a plurality of macro output primitives.

32. A electronic design automation system as recited in Claim 28 wherein said memory is a content addressable memory (CAM) and wherein said plurality of ATPG memory primitives comprises:

a memory primitive;

a compare port primitive for coupling to receive coupled first data from a data bus primitive and for coupling to said receive second data from said memory primitive, wherein said compare port primitive is for comparing said first data and said second data and for supplying an address of said memory primitive provided said first data matches said second data; and

a plurality of macro output primitives for outputting said address of said memory primitive.

33. A electronic design automation system as recited in Claim 25 wherein said method further comprises the step of verifying functional equivalence between said simplified behavioral model and said simulation model by applying both models to a behavioral hardware description language simulator.

34. A electronic design automation system as recited in Claim 25 wherein said behavioral hardware description language is Verilog.

35. A electronic design automation system as recited in Claim 25 wherein said behavioral hardware description language is VHDL.

36. A electronic design automation system as recited in Claim 25 further comprises the step of displaying a graphical representation of said

primitives of said structural model of said memory and their interconnections ~~on~~ said display device.